Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A manufacturing method of a semiconductor integrated circuit device, comprising the steps of:

(a) forming ordinary interconnections on a first major surface of a wafer;

(b) forming re-interconnections including plural first metal film regions and plural second metal film regions over the ordinary interconnections;

(c) forming a polymeric resin film over the re-interconnections;

(d) forming plural first metal pad regions and plural second metal pad regions by forming openings through portions of the polymeric resin film which correspond to the first metal film regions and the second metal film regions, respectively, by a lithography technique;

(e) forming bumps on the respective first metal pad regions;

(f) after the step (e), dividing the wafer into plural semiconductor integrated circuit chips;

(g) causing a bump formation surface, corresponding to the first major surface of the wafer, of a first semiconductor integrated circuit chip among the plural divisional semiconductor integrated circuit chips to be opposed to an electrode surface of a burn-in test socket, and performing a burn-in test in a state that the plural bumps on the bump formation surface and plural metal projection electrodes on the electrode surface are pressed against each other; and

(h) after the step (g), separating the metal projection electrodes and the bumps of the first semiconductor integrated circuit chip from each other by pushing at least

one of the plural second metal pad regions on the bump formation surface in such a direction that the first semiconductor integrated circuit chip and the electrode surface go away from each other by bringing at least one pushing member whose contact surface is narrower than the at least one second metal pad region into contact with the at least one second metal pad region.

2. (Original) The manufacturing method of a semiconductor integrated circuit device according to claim 1, wherein the polymeric resin film contains a thermosetting resin as a main component.

3. (Original) The manufacturing method of a semiconductor integrated circuit device according to claim 1, wherein the polymeric resin film contains a heat-resistant thermosetting resin as a main component.

4. (Original) The manufacturing method of a semiconductor integrated circuit device according to claim 1, wherein the polymeric resin film contains a polyimide resin as a main component.

5. (Original) The manufacturing method of a semiconductor integrated circuit device according to claim 1, wherein the polymeric resin film contains an organic thermosetting resin as a main component.

6. (Original) The manufacturing method of a semiconductor integrated circuit device according to claim 1, wherein a pitch of the bumps is smaller than 500 μm.

7. (Original) The manufacturing method of a semiconductor integrated circuit device according to claim 1, wherein the bumps are formed by a lithography technique or a printing technique.

8. (Original) The manufacturing method of a semiconductor integrated circuit device according to claim 1, wherein a ratio of a height to a diameter of the bumps in terms of an average ratio of completed bumps in the chip is smaller than 60%.

9. (Original) The manufacturing method of a semiconductor integrated circuit device according to claim 1, wherein the number of at least one second metal pad region in the first semiconductor integrated circuit chip is two or more.

10. (Original) The manufacturing method of a semiconductor integrated circuit device according to claim 1, wherein the number of at least one second metal pad region in the first semiconductor integrated circuit chip is three or more.

11. (Original) The manufacturing method of a semiconductor integrated circuit device according to claim 1, wherein the at least one second metal pad region in the first semiconductor integrated circuit chip is provided in a chip peripheral portion of the bump formation surface of the first semiconductor integrated circuit chip.

12. (Original) The manufacturing method of a semiconductor integrated circuit device according to claim 1, wherein the at least one second metal pad region in the first semiconductor integrated circuit chip is provided in a chip corner portion of the bump formation surface of the first semiconductor integrated circuit chip.

13. (Original) The manufacturing method of a semiconductor integrated circuit device according to claim 1, wherein the at least one second metal pad region in the first semiconductor integrated circuit chip is in an electrically floating state.

14. (Original) The manufacturing method of a semiconductor integrated circuit device according to claim 1, wherein an area of each of the second metal pad regions is larger than that of each of the first metal pad regions.

15. (Original) The manufacturing method of a semiconductor integrated circuit device according to claim 1, wherein an area of each of the second metal pad regions is two times or more larger than that of each of the first metal pad regions.

16. (Original) The manufacturing method of a semiconductor integrated circuit device according to claim 1, wherein an area of each of the second metal pad regions is three times or more larger than that of each of the first metal pad regions.

17. (Original) The manufacturing method of a semiconductor integrated circuit device according to claim 1, wherein an area of the contact surface of each of the at least one pushing member is two times or more larger than that of each of the first metal pad regions.

18. (Original) The manufacturing method of a semiconductor integrated circuit device according to claim 1, wherein the at least one pushing member is not brought into contact with a top surface of the polymeric resin film.

19. (Original) The manufacturing method of a semiconductor integrated circuit device according to claim 1, wherein each of the metal projection electrodes is formed by forming a plating layer having gold as a main component on a core member having nickel as a main component.

20. (Original) The manufacturing method of a semiconductor integrated circuit device according to claim 19, wherein each of the metal projection electrodes is formed by further plating, with rhodium, the plating layer having gold as the main component.

21. (New) The manufacturing method of a semiconductor integrated circuit device according to claim 18, wherein the polymeric resin film contains a polyimide resin as a main component.

22. (New) The manufacturing method of a semiconductor integrated circuit device according to claim 18, wherein the number of at least one second metal pad region in the first semiconductor integrated circuit chip is three or more.

23. (New) The manufacturing method of a semiconductor integrated circuit device according to claim 18, wherein the at least one second metal pad region in the first semiconductor integrated circuit chip is provided in a chip corner portion of the bump formation surface of the first semiconductor integrated circuit chip.

24. The manufacturing method of a semiconductor integrated circuit device according to claim 23, wherein the number of at least one second metal pad region in the first semiconductor integrated circuit chip is three or more.

25. (New) The manufacturing method of a semiconductor integrated circuit device according to claim 24, wherein the at least one second metal pad region in the first semiconductor integrated circuit chip is provided in a chip corner portion of the bump formation surface of the first semiconductor integrated circuit chip.

26. (New) The manufacturing method of a semiconductor integrated circuit device according to claim 25, wherein the polymeric resin film contains a polyimide resin as a main component.